WHAT IS CLAIMED IS:

1. A light emitting device comprising:

a plurality of pixels each having an electro luminescence element, said electro luminescence element comprising:

a pixel electrode;

an opposing electrode; and

an electro luminescence layer provided between the pixel electrode and the opposing electrode,

wherein said pixels are arranged in lines and the opposing electrode of the electro luminescence element is connected to other opposing electrodes that are on the same line, and

wherein electric potential of the pixel electrode is controlled by a digital video signal.

2. A device according to claim 1, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

3. A device according to claim 2, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

4. A device according to claim 2, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

5.A device according to claim 1, wherein the light emitting device is a computer.

6. A device according to claim 1, wherein the light emitting device is a video camera.

7. A device according to claim 1, wherein the light emitting device is a DVD player.

8. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit; and

a pixel portion having a plurality of pixels, each pixel comprising:

an electro luminescence element;

a switching TFT; and

an electro luminescence driver TFT,

wherein said electro luminescence element comprises a pixel electrode, an opposing electrode, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

wherein electric potential of the opposing electrode is controlled by the opposing power source line driver circuit;

wherein the gate signal line driver circuit controls drive of the switching TFT;

wherein the switching TFT controls drive of the electro luminescence driver TFT; and

wherein the electro luminescence driver TFT controls the electric potential of the pixel electrode.

9. A device according to claim 8, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

10. A device according to claim 9, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

11. A device according to claim 9, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

12. A device according to claim 8, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

13. A device according to claim 8, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

14.A device according to claim 8, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

15. A device according to claim 14, wherein the bank has a light-shielding property.

16.A device according to claim 8, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

17. A device according to claim 8, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

18.A device according to claim 8, wherein the electro luminescence driver TFT is driven in a linear range.

19.A device according to claim 8, wherein the light emitting device is a computer.

20. A device according to claim 8, wherein the light emitting device is a video camera.

21. A device according to claim 8, wherein the light emitting device is a DVD player.

22. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit; and

a pixel portion having a plurality of pixels, each pixel having an electro luminescence element, a switching TFT and an electro luminescence driver TFT,

wherein the electro luminescence element comprises a pixel electrode, an opposing electrode, and an electro luminescence layer provided between the pixel electrode and the opposing electrode,

wherein the gate signal line driver circuit controls drive of the switching TFT,

wherein the switching TFT controls drive of the electro luminescence driver TFT, and

wherein the electro luminescence driver TFT controls the electric potential of the pixel electrode and the electric potential of the opposing electrode is controlled by the opposing power source line driver circuit, to thereby control the length of time during which the electro luminescence element emits light for gray scale display.

23. A device according to claim 22, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

24. A device according to claim 23, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

25. A device according to claim 23, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

26. A device according to claim 22, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

27. A device according to claim 22, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

28.A device according to claim 22, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

29. A device according to claim 28, wherein the bank has a light-shielding property.

30.A device according to claim 22, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

31. A device according to claim 22, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

32.A device according to claim 22, wherein the electro luminescence driver TFT is driven in a linear range.

33.A device according to claim 22, wherein the light emitting device is a computer.

34. A device according to claim 22, wherein the light emitting device is a video camera.

35. A device according to claim 22, wherein the light emitting device is a DVD player.

36. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit;

a pixel portion comprising a plurality of pixels;

a plurality of source signal lines connected to the source signal line driver circuit;

a plurality of gate signal lines connected to the gate signal line driver circuit;

a plurality of opposing power source lines connected to the opposing power source line driver circuit; and

a plurality of power source supply lines,

wherein each pixel comprises:

a switching TFT having a gate electrode connected to any one of the plural gate signal lines, and a source region and a drain region one of which is connected to any one of the plural source signal lines;

an electro luminescence driver TFT, a gate electrode of said electro luminescence driver TFT connected to the other of said source region and said drain region of switching TFT;

an electro luminescence element comprises a pixel electrode, an opposing electrode connected to any one of the plural opposing power source lines, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

wherein the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines, and the electro luminescence driver TFT has a drain region connected to the pixel electrode.

37. A device according to claim 36, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

38. A device according to claim 37, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

39. A device according to claim 37, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

40. A device according to claim 36, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

41. A device according to claim 36, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

42.A device according to claim 36, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

43. A device according to claim 42, wherein the bank has a light-shielding property.

44.A device according to claim 36, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

45. A device according to claim 36, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

46.A device according to claim 36, wherein the electro luminescence driver TFT is driven in a linear range.

47.A device according to claim 36, wherein the light emitting device is a computer.

48. A device according to claim 36, wherein the light emitting device is a video camera.

49. A device according to claim 36, wherein the light emitting device is a DVD player.

50. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit;

a pixel portion having a plurality of pixels, each pixel comprising a switching TFT, an electro luminescence driver TFT and an electro luminescence element;

a plurality of source signal lines connected to the source signal line driver circuit;

a plurality of gate signal lines connected to the gate signal line driver circuit;

a plurality of opposing power source lines connected to the opposing power source line driver circuit; and

a plurality of power source supply lines,

wherein the switching TFT comprises a gate electrode connected to any one of the plural gate signal lines, and the switching TFT comprising a source region and

a drain region one of which is connected to any one of the plural source signal lines and the other of which is connected to a gate electrode of the electro luminescence driver TFT;

the electro luminescence element comprises a pixel electrode, an opposing electrode whose electric potential is kept constant, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines, and the electro luminescence driver TFT has a drain region connected to the pixel electrode; and

the opposing electrode is connected to any one of the plural opposing power source lines.

51. A device according to claim 50, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

52. A device according to claim 51, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

53. A device according to claim 51, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

54. A device according to claim 50, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

55. A device according to claim 50, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

56.A device according to claim 50, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

57. A device according to claim 56, wherein the bank has a light-shielding property.

58.A device according to claim 50, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

59. A device according to claim 50, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

60. A device according to claim 50, wherein the electro luminescence driver TFT is driven in a linear range.

61.A device according to claim 50, wherein the light emitting device is a computer.

62. A device according to claim 50, wherein the light emitting device is a video camera.

63. A device according to claim 50, wherein the light emitting device is a DVD player.

64. A light emitting device comprising a source signal line driver circuit, a gate signal line driver circuit, an opposing power source line driver circuit and a pixel portion, wherein:

the pixel portion has a plurality of pixels;

the plural pixels each have an electro luminescence element, a switching TFT and an electro luminescence driver TFT;

the electro luminescence element is composed of a pixel electrode, an opposing electrode, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

the electric potential of the opposing electrode is controlled by the opposing power source line driver circuit;

the gate signal line driver circuit controls drive of the switching TFT;

the switching TFT controls drive of the electro luminescence driver TFT;

the electro luminescence driver TFT controls the electric potential of the pixel electrode;

for each pixel on the respective lines in the pixel portion, one frame period has n display periods Tr1, Tr2, ... and Trn and has j non-display periods Td1, Td2, ... and Tdj;

Tri (i = 1, ..., n) is an arbitrary display period chosen out of the n display periods Tr1, Tr2, ... and Trn; Tai is an arbitrary writing period chosen out of n writing periods Ta1, Ta2, ... and Tan; Tek (k = 1, ..., j) is an arbitrary erasing period chosen out of j erasing periods Te1, Te2, ... and Tej; and the arbitrary display period Tri is defined as a period which starts as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the wiring period Tai and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the writing period Tai in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential, the arbitrary display period Tri alternatively ending as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek;

Tdk is an arbitrary non-display period chosen out of the j non-display periods Td1, Td2, ... and Tdj, and the arbitrary non-display period Tdk is defined as a period which starts as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the erasing period Tek in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro

luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential;

any one of the n writing periods Ta1, Ta2, ... and Tan partially overlaps with one or two of the j erasing periods Te1, Te2, ... and Tej;

when all of the n writing periods Ta1, Ta2, ... and Tan have come and gone, any one of the n writing periods Ta1, Ta2, ... and Tan comes again;

the digital video signal determines whether or not the El element emits light during the n display periods Tr1, Tr2, ... and Trn; and

the ratio of the length of the n display periods Tr1, Tr2, ... and Trn is expressed as $2^0 : 2^1 : ... : 2^{(n-1)}$.

65. A device according to claim 64, wherein the longest non-display period out of the non-display periods Td1, Td2, ... and Tdj comes last in the frame period.

66. A device according to claim 64, wherein the writing periods Ta1, Ta2, ... and Tan do not overlap with one another.

67. A device according to claim 64, wherein the erasing periods Te1, Te2, ... and Tej do not overlap with one another.

68. A device according to claim 64, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

69. A device according to claim 68, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

70. A device according to claim 68, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

71. A device according to claim 64, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

72. A device according to claim 64, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

73.A device according to claim 64, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

74. A device according to claim 73, wherein the bank has a light-shielding property.

75.A device according to claim 64, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

76. A device according to claim 64, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

77.A device according to claim 64, wherein the electro luminescence driver TFT is driven in a linear range.

78.A device according to claim 64, wherein the light emitting device is a computer.

79. A device according to claim 64, wherein the light emitting device is a video camera.

80. A device according to claim 64, wherein the light emitting device is a DVD player.

81. A light emitting device comprising a source signal line driver circuit, a gate signal line driver circuit, an opposing power source line driver circuit and a pixel portion, wherein:

the pixel portion has a plurality of pixels;

the plural pixels each have an electro luminescence element, a switching TFT and an electro luminescence driver TFT;

the electro luminescence element is composed of a pixel electrode, an opposing electrode, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

the gate signal line driver circuit controls drive of the switching TFT;

the switching TFT controls drive of the electro luminescence driver TFT;

the electro luminescence driver TFT controls the electric potential of the pixel electrode and the electric potential of the opposing electrode is controlled by the

opposing power source line driver circuit, to thereby control the length of time during which the electro luminescence element emits light for gray scale display;

for each pixel on the respective lines in the pixel portion, one frame period has n display periods Tr1, Tr2, ... and Trn and has j non-display periods Td1, Td2, ... and Tdj;

Tri (i = 1, ..., n) is an arbitrary display period chosen out of the n display periods Tr1, Tr2, ... and Trn; Tai is an arbitrary writing period chosen out of n writing periods Ta1, Ta2, ... and Tan; Tek (k = 1, ..., j) is an arbitrary erasing period chosen out of j erasing periods Te1, Te2, ... and Tej; and the arbitrary display period Tri is defined as a period which starts as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the wiring period Tai and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the writing period Tai in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential, the arbitrary display period Tri alternatively ending as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek;

Tdk is an arbitrary non-display period chosen out of the j non-display periods Td1, Td2, ... and Tdj, and the arbitrary non-display period Tdk is defined as a period which starts as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF

opposing electric potential during the erasing period Tek and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the erasing period Tek in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential;

any one of the n writing periods Ta1, Ta2, ... and Tan partially overlaps with one or two of the j erasing periods Te1, Te2, ... and Tej;

when all of the n writing periods Ta1, Ta2, ... and Tan have come and gone, any one of the n writing periods Ta1, Ta2, ... and Tan comes again;

the digital video signal determines whether or not the El element emits light during the n display periods Tr1, Tr2, ... and Trn; and

the ratio of the length of the n display periods Tr1, Tr2, ... and Trn is expressed as $2^0 : 2^1 : \ldots : 2^{(n-1)}$.

82. A device according to claim 81, wherein the longest non-display period out of the non-display periods Td1, Td2, ... and Tdj comes last in the frame period.

83. A device according to claim 81, wherein the writing periods Ta1, Ta2, ... and Tan do not overlap with one another.

84. A device according to claim 81, wherein the erasing periods Te1, Te2, ... and Tej do not overlap with one another.

85. A device according to claim 81, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

86. A device according to claim 85, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

87. A device according to claim 85, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

88. A device according to claim 81, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

89. A device according to claim 81, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

90. A device according to claim 81, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

91 A device according to claim 90, wherein the bank has a light-shielding property.

92.A device according to claim 81, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

93. A device according to claim 81, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

94.A device according to claim 81, wherein the electro luminescence driver TFT is driven in a linear range.

95.A device according to claim 81, wherein the light emitting device is a computer.

96. A device according to claim 81, wherein the light emitting device is a video camera.

97. A device according to claim 81, wherein the light emitting device is a DVD player.

98. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit;

a pixel portion;

a plurality of source signal lines connected to the source signal line driver circuit;

a plurality of gate signal lines connected to the gate signal line driver circuit;

a plurality of opposing power source lines connected to the opposing power source line driver circuit; and

a plurality of power source supply lines, wherein:

the pixel portion has a plurality of pixels;

the plural pixels each have a switching TFT, an electro luminescence driver TFT and an electro luminescence element;

the switching TFT has a gate electrode connected to any one of the plural gate signal lines, and the switching TFT has a source region and a drain region one of which is connected to any one of the plural source signal lines and the other of which is connected to a gate electrode of the electro luminescence driver TFT;

the electro luminescence element is composed of a pixel electrode, an opposing electrode, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines, and the electro luminescence driver TFT has a drain region connected to the pixel electrode;

the opposing electrode is connected to any one of the plural opposing power source lines;

for each pixel on the respective lines in the pixel portion, one frame period has n display periods Tr1, Tr2, ... and Trn and has j non-display periods Td1, Td2, ... and Tdj;

Tri (i = 1, ..., n) is an arbitrary display period chosen out of the n display periods Tr1, Tr2, ... and Trn; Tai is an arbitrary writing period chosen out of n writing

periods Ta1, Ta2, ... and Tan; Tek (k = 1, ..., j) is an arbitrary erasing period chosen out of j erasing periods Te1, Te2, ... and Tej; and the arbitrary display period Tri is defined as a period which starts as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the wiring period Tai and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the writing period Tai in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential, the arbitrary display period Tri alternatively ending as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek;

Tdk is an arbitrary non-display period chosen out of the j non-display periods Td1, Td2, ... and Tdj, and the arbitrary non-display period Tdk is defined as a period which starts as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the erasing period Tek in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential;

any one of the n writing periods Ta1, Ta2, ... and Tan partially overlaps with one or two of the j erasing periods Te1, Te2, ... and Tej;

when all of the n writing periods Ta1, Ta2, ... and Tan have come and gone, any one of the n writing periods Ta1, Ta2, ... and Tan comes again;

the digital video signal determines whether or not the El element emits light during the n display periods Tr1, Tr2, ... and Trn; and

the ratio of the length of the n display periods Tr1, Tr2, ... and Trn is expressed as $2^0 : 2^1 : ... : 2^{(n-1)}$.

99. A device according to claim 98, wherein the longest non-display period out of the non-display periods Td1, Td2, ... and Tdj comes last in the frame period.

100. A device according to claim 98, wherein the writing periods Ta1, Ta2, ... and Tan do not overlap with one another.

101. A device according to claim 98, wherein the erasing periods Te1, Te2, ... and Tej do not overlap with one another.

102. A device according to claim 98, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

103. A device according to claim 102, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

104. A device according to claim 102, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

105. A device according to claim 98, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

106. A device according to claim 98, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

107. A device according to claim 98, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

108. A device according to claim 107, wherein the bank has a light-shielding property.

109. A device according to claim 98, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

110. A device according to claim 98, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

111.A device according to claim 98, wherein the electro luminescence driver TFT is driven in a linear range.

112.A device according to claim 98, wherein the light emitting device is a computer.

113. A device according to claim 98, wherein the light emitting device is a video camera.

114. A device according to claim 98, wherein the light emitting device is a DVD player.

115. A light emitting device comprising:

a source signal line driver circuit;

a gate signal line driver circuit;

an opposing power source line driver circuit;

a pixel portion;

a plurality of source signal lines connected to the source signal line driver circuit;

a plurality of gate signal lines connected to the gate signal line driver circuit;

a plurality of opposing power source lines connected to the opposing power source line driver circuit; and

a plurality of power source supply lines, wherein:

the pixel portion has a plurality of pixels;

the plural pixels each have a switching TFT, an electro luminescence driver TFT and an electro luminescence element;

the switching TFT has a gate electrode connected to any one of the plural gate signal lines, and the switching TFT has a source region and a drain region one of which is connected to any one of the plural source signal lines and the other of which is connected to a gate electrode of the electro luminescence driver TFT;

the electro luminescence element is composed of a pixel electrode, an opposing electrode whose electric potential is kept constant, and an electro luminescence layer provided between the pixel electrode and the opposing electrode;

the electro luminescence driver TFT has a source region connected to any one of the plural power source supply lines, and the electro luminescence driver TFT has a drain region connected to the pixel electrode;

the opposing electrode is connected to any one of the plural opposing power source lines;

for each pixel on the respective lines in the pixel portion, one frame period has n display periods Tr1, Tr2, ... and Trn and has j non-display periods Td1, Td2, ... and Tdj;

Tri (i = 1, ..., n) is an arbitrary display period chosen out of the n display periods Tr1, Tr2, ... and Trn; Tai is an arbitrary writing period chosen out of n writing periods Ta1, Ta2, ... and Tan; Tek (k = 1, ..., j) is an arbitrary erasing period chosen out of j erasing periods Te1, Te2, ... and Tej; and the arbitrary display period Tri is defined as a period which starts as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the wiring period Tai and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in

the pixel portion receive an ON opposing electric potential and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the writing period Tai in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential, the arbitrary display period Tri alternatively ending as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek;

Tdk is an arbitrary non-display period chosen out of the j non-display periods Td1, Td2, ... and Tdj, and the arbitrary non-display period Tdk is defined as a period which starts as all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an OFF opposing electric potential during the erasing period Tek and which ends as a digital video signal is inputted to the pixels on the respective lines in the pixel portion during the next writing period that comes next to the erasing period Tek in the n writing periods Ta1, Ta2, ... and Tan and all the opposing electrodes of the electro luminescence elements of the pixels on the respective lines in the pixel portion receive an ON opposing electric potential;

any one of the n writing periods Ta1, Ta2, ... and Tan partially overlaps with one or two of the j erasing periods Te1, Te2, ... and Tej;

when all of the n writing periods Ta1, Ta2, ... and Tan have come and gone, any one of the n writing periods Ta1, Ta2, ... and Tan comes again;

the digital video signal determines whether or not the El element emits light during the n display periods Tr1, Tr2, ... and Trn; and

the ratio of the length of the n display periods Tr1, Tr2, ... and Trn is expressed as $2^0 : 2^1 : \ldots : 2^{(n-1)}$.

116. A device according to claim 115, wherein the longest non-display period out of the non-display periods Td1, Td2, ... and Tdj comes last in the frame period.

117. A device according to claim 115, wherein the writing periods Ta1, Ta2, ... and Tan do not overlap with one another.

118. A device according to claim 115, wherein the erasing periods Te1, Te2, ... and Tej do not overlap with one another.

119. A device according to claim 115, wherein the electro luminescence layer is formed of a monomer organic material or a polymer organic material.

120. A device according to claim 119, wherein the monomer organic material comprises Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

121. A device according to claim 119, wherein the polymer organic material comprises PPV (polyphenylene vinylene), PVK (polyvinyl carvazole) or polycarbonate.

122. A device according to claim 115, wherein, when the pixel electrode is an anode, the electro luminescence driver TFT is a p-channel TFT.

123. A device according to claim 115, wherein, when the pixel electrode is a cathode, the electro luminescence driver TFT is an n-channel TFT.

124.A device according to claim 115, wherein the pixel electrode is connected to the drain region of the electro luminescence driver TFT directly or through at least one wiring, and

wherein a bank is formed on a region where the pixel electrode is connected to the drain region of the electro luminescence driver TFT, or on a region where the pixel electrode is connected to at least one wiring.

125. A device according to claim 124, wherein the bank has a light-shielding property.

126.A device according to claim 115, wherein the switching TFT or the electro luminescence driver TFT is of top gate type.

127. A device according to claim 115, wherein the switching TFT or the electro luminescence driver TFT is of bottom gate type.

128. A device according to claim 115, wherein the electro luminescence driver TFT is driven in a linear range.

129.A device according to claim 115, wherein the light emitting device is a computer.

130. A device according to claim 115, wherein the light emitting device is a video camera.

131. A device according to claim 115, wherein the light emitting device is a DVD player.